AMENDMENTS TO THE SPECIFICATION

Please amend Paragraphs [0010], [0015], [0019], [0063] and [0090] of the specification as follows:

[0010] Numerous patents and applications assigned to or in the names of the Massachusetts Institute of Technology (MIT) and E Ink Corporation have recently been published describing encapsulated electrophoretic media. Such encapsulated media comprise numerous small capsules, each of which itself comprises an internal phase containing electrophoretically-mobile particles suspended in a liquid suspension medium, and a capsule wall surrounding the internal phase. Typically, the capsules are themselves held within a polymeric binder to form a coherent layer positioned between two electrodes. Encapsulated media of this type are described, for example, in U.S. Patents Nos. 5,930,026; 5,961,804; 6,017,584; 6,067,185; 6,118,426; 6,120,588; 6,120,839; 6,124,851; 6,130,773; 6,130,774; 6,172,798; 6,177,921; 6,232,950; [[6,249,721]]6,249,271; 6,252,564; 6,262,706; 6,262,833; 6,300,932; 6,312,304; 6,312,971; 6,323,989; 6,327,072; 6,376,828; 6,377,387; 6,392,785; 6,392,786; 6,413,790; 6,422,687; 6,445,374; 6,445,489; 6,459,418; 6,473,072; 6,480,182; 6,498,114; 6,504,524; 6,506,438; 6,512,354; 6,515,649; 6,518,949; 6,521,489; 6,531,997; 6,535,197; 6,538,801; 6,545,291; 6,580,545; 6,639,578; 6,652,075; and 6,657,772; and U.S. patent applications Publication Nos. 2002/0019081; 2002/0021270; 2002/0053900; 2002/0060321; 2002/0063661; 2002/0063677; 2002/0090980; 2002/0106847; 2002/0113770; 2002/0130832; 2002/0131147; 2002/0145792; 2002/0171910; 2002/0180687; 2002/0180688; 2002/0185378; 2003/0011560; 2003/0011868; 2003/0020844; 2003/0025855; 2003/0034949; 2003/0038755; 2003/0053189; 2003/0076573; 2003/0096113; 2003/0102858; 2003/0132908; 2003/0137521; 2003/0137717; 2003/0151702; and 2003/0214697 and International Applications Publication Nos. WO 99/67678; WO 00/05704; WO 00/38000; WO 00/38001; WO 00/36560; WO 00/67110; WO 00/67327; WO 01/07961; and WO 01/08241.

[0015] Obviously, in order for an electro-optic display to operate, it is necessary to arrange for the provision of controllable electric fields across the electro-optic medium to switch the medium among its various optical states, and thus to arrange electrodes on both sides of the medium. In the simplest form of display, each pixel of the display is associated with a separate electrode provided with its own switchable connection to various voltage levels. However, in a high resolution display, for example a VGA (640 x 480) display, this architecture becomes impracticable because of the enormous number of electrical leads required. Accordingly, it is common in such displays to use an active matrix display architecture which has a single common, transparent electrode on one side of the electro-optic layer, this common electrode extending across all the pixels of the display. Typically, this common electrode lies between the electro-optic layer and the observer and forms a viewing surface through which an observer views the display. On the opposed side of the electro-optic layer is disposed a matrix of pixel electrodes arranged in rows and columns such that each pixel electrode is uniquely defined by the intersection of a single row and a single column. Thus, the electric field experienced by each pixel of the electro-optic layer is controlled by varying the voltage applied to the associated pixel electrode relative to the voltage applied to the common front electrode. Each pixel electrode is associated with at least one non-linear device, typically a thin film transistor, although diodes can also be used. The gates of the transistors in each row are connected via a single elongate row electrode to a row driver. The source electrodes of the transistors in each column are connected via a single elongate column electrode to a column driver. The drain electrode of each transistor is connected directly to the pixel electrode. It will be appreciated that the assignment of the gates to rows and the source electrodes to columns is arbitrary, and could be reversed, as could the assignment of source and drain electrodes. The array of non-linear devices and their associated row and column electrodes form the backplane of the display; typically, this backplane will include the row and column driver circuitry in the same physical unit. In many electro-optic displays, an active matrix architecture allows the relatively complex backplane to

be fabricated separately from the remainder of the display using conventional semiconductor fabrication techniques. The remainder, or front portion, of the display may, for example, be fabricated inexpensively by depositing a layer of electro-optic medium on a polymeric film on which has previously been deposited a substantially transparent conductive layer, formed, for example, from indium tin oxide (ITO) or an organic polymeric conductor. The front portion of the display is then typically laminated to the backplane.

[0019] This aspect of the invention may hereinafter for convenience be referred to as the MicroElectroMechanical System ("MEMS") backplane of the invention. In one form of such a MEMS backplane, the micromechanical switch comprises a cantilever beam capable [[on]]of moving into and out of contact with a first electrode, and a second electrode arranged to move the cantilever beam. Such a MEMS backplane may further comprise a capacitor electrode disposed adjacent the first electrode such that the capacitor electrode and the first electrode form a capacitor. A MEMS backplane may be provided with an encapsulant layer covering the micromechanical switch.

[0063] The MEMS backplane of the present invention reduces or eliminates these problems of prior art backplanes. A preferred form of such a MEMS backplane for an electro-optic display has a plurality of ~~MicroElectroMechanical System (~~MEMS[[)]] switches and is useful for addressing a flat panel display, such as an electrophoretic display.

[0090] To avoid such problems, it is known to interpose a barrier or passivation layer between the non-linear devices and the electro-optic medium. For example, ~~the aforementioned~~ US Patent Application Publication No. 2002/0119584 describes a backplane having a so-called "buried transistor design". In such a design, only the pixel electrodes are exposed upon the surface of final backplane prior to lamination; the transistors of the backplane are "buried" underneath a passivation layer, with the drains of the transistors being connected to their associated pixel electrodes by conductive vias passing through the passivation layer. In the preferred form of this design as described in

the aforementioned published application, the passivation layer comprises more than about 5 μm of silicon nitride deposited by plasma enhanced chemical vapor deposition (PECVD), and this relatively thick layer must cover both the channels of the transistors and the data lines. It is difficult if not impossible to deposit such a thick nitride layer without cracking. Accordingly, it is desirable to find an alternative material to replace the silicon nitride as the passivation layer.